MEMORY CELL STRUCTURE OF METAL PROGRAMMABLE READ ONLY MEMORY HAVING BIT CELLS WITH A SHARED TRANSISTOR CELL

ABSTRACT OF DISCLOSURE

A memory cell structure of a metal (or via) programmable ROM whereby a transistor is shared between bit cells of the programmable ROM. Such a memory cell structure may include: a word line; a bit line; first and second virtual grounding lines; a grounding line; a first bit cell selected by signals of the word line and the first virtual grounding line; and a second bit cell selected by signals of the word line and the second virtual grounding line, wherein a cell transistor, one side of which is connected to the bit line is shared both by the first and second bit cells. Also, the other side of the cell transistor may be floated or connected to the bit line or, alternatively, connected to any one of the first virtual grounding line, the second virtual grounding line and the grounding line, and the gate of the cell transistor is connected to the word line.